In re Patent Application of
PEZZINI
Serial No. **Not Yet Assigned**
Filed: **Herewith**
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In the Claims:

Claims 1-7 (Cancelled).

8. (New) An integrated circuit comprising:

at least one input pad for receiving an externally generated analog signal;

pre-sampling means for pre-sampling at least one internally generated analog reference signal;

an analog-to-digital converter connected to said at least one input pad for providing a numerical value of the externally generated analog signal, and connected to said pre-sampling means for providing a numerical value of the internally generated analog reference signal; and

fault signaling means connected to said pre-sampling means and to said analog-to-digital converter for generating a fault signal when the numerical value of the externally generated analog signal is equal to the numerical value of the internally generated analog reference signal, the fault signal indicating that an electrical connection providing the externally generated analog signal to said at least one input pad is faulty.

9. (New) An integrated circuit according to Claim 8, wherein said analog-to-digital converter comprises a successive approximations analog-to-digital converter.

10. (New) An integrated circuit according to Claim 8, wherein said pre-sampling means comprises:

a biasing stage for providing the at least one internally generated analog reference signal; and

a pair of input path selection switches coupling the

input of said analog-to-digital converter either to an output of said biasing stage during a pre-sampling phase of said analog-to-digital converter or to said at least one input pad during a successive operating phase of said analog-to-digital converter;

said fault signaling means comprising logic control circuitry for driving said pair of input path selection switches.

11. (New) An integrated circuit according to Claim 10, wherein said fault signaling means further comprises:

a register for storing the numerical value of the internally generated analog reference signal;

a comparator having a first input connected to said register for receiving the numerical value of the internally generated analog reference signal, and a second input connected to said analog-to-digital converter for receiving the numerical value of the externally generated analog signal; and

a pair of output path selection switches coupling an output of said analog-to-digital converter either to an input of said register during the pre-sampling phase of said analog-to-digital converter or to the second input of said comparator during the successive operating phase of the analog-to-digital converter;

said logic control circuitry for driving said pair of output path selection switches.

12. (New) An integrated circuit according to Claim 11, wherein an output of said comparator provides the fault signal.

13. (New) An integrated circuit according to Claim 11, wherein said logic control circuitry drives said pair of input path selection switches in an opposing phase, and drives said pair of output path selection switches in an opposing phase.

14. (New) An integrated circuit according to Claim 11, wherein said comparator defines a range of values between two thresholds for comparing with the numerical value of the externally generated analog signal.

15. (New) An integrated circuit according to Claim 11, wherein said fault detection means further comprises a counter coupled to an output of said comparator for providing the fault signal when said comparator verifies that the numerical value of the externally generated analog signal is equal to the numerical value of the internally generated analog reference signal for a certain number of successive samples of the externally generated analog input signal.

16. (New) An integrated circuit comprising:

at least one input pad for receiving an externally generated analog signal;

a pre-sampling circuit for pre-sampling at least one internally generated analog reference signal;

an analog-to-digital converter connected to said at least one input pad for providing a numerical value of the externally generated analog signal, and connected to said pre-sampling circuit for providing a numerical value of the internally generated analog reference signal; and

a fault signaling circuit connected to said pre-sampling circuit and to said analog-to-digital converter for generating a fault signal when the numerical value of the externally generated analog signal is equal to the numerical value of the internally generated analog reference signal.

17. (New) An integrated circuit according to Claim 16, wherein said analog-to-digital converter comprises a successive approximations analog-to-digital converter.

18. (New) An integrated circuit according to Claim 16, wherein said pre-sampling circuit comprises:

a biasing stage for providing the at least one internally generated analog reference signal; and

a pair of input path selection switches coupling the input of said analog-to-digital converter either to an output of said biasing stage during a pre-sampling phase of said analog-to-digital converter or to said at least one input pad during a successive operating phase of said analog-to-digital converter;

said fault signaling circuit comprising logic control circuitry for driving said pair of input path selection switches.

19. (New) An integrated circuit according to Claim 18, wherein said fault signaling circuit further comprises:

a register for storing the numerical value of the internally generated analog reference signal;

a comparator having a first input connected to said register for receiving the numerical value of the internally generated analog reference signal, and a second input

connected to said analog-to-digital converter for receiving the numerical value of the externally generated analog signal; and

a pair of output path selection switches coupling an output of said analog-to-digital converter either to an input of said register during the pre-sampling phase of said analog-to-digital converter or to the second input of said comparator during the successive operating phase of the analog-to-digital converter;

said logic control circuitry for driving said pair of output path selection switches.

20. (New) An integrated circuit according to Claim 19, wherein an output of said comparator provides the fault signal.

21. (New) An integrated circuit according to Claim 19, wherein said logic control circuitry drives said pair of input path selection switches in an opposing phase, and drives said pair of output path selection switches in an opposing phase.

22. (New) An integrated circuit according to Claim 19, wherein said comparator defines a range of values between two thresholds for comparing with the numerical value of the externally generated analog signal.

23. (New) An integrated circuit according to Claim 19, wherein said fault detection circuit further comprises a counter coupled to an output of said comparator for providing the fault signal when said comparator verifies that the

numerical value of the externally generated analog signal is equal to the numerical value of the internally generated analog reference signal for a certain number of successive samples of the externally generated analog input signal.

24. (New) A method for indicating if an electrical connection providing an externally generated analog signal to at least one input of an integrated circuit is faulty, the method comprising:

providing the externally generated analog signal to the at least one input pad of the integrated circuit;

pre-sampling at least one internally generated analog reference signal;

providing a numerical value of the externally generated analog signal and a numerical value of the internally generated analog reference signal using an analog-to-digital converter; and

generating a fault signal when the numerical value of the externally generated analog signal is equal to the numerical value of the internally generated analog reference signal.

25. (New) A method according to Claim 24, wherein the analog-to-digital converter comprises a successive approximations analog-to-digital converter.

26. (New) A method according to Claim 24, wherein the pre-sampling is performed using a pre-sampling circuit comprising a biasing stage for providing the at least one internally generated analog reference signal; and a pair of input path selection switches coupling the input of the

analog-to-digital converter either to an output of the biasing stage during a pre-sampling phase of the analog-to-digital converter or to the at least one input pad during a successive operating phase of the analog-to-digital converter; and wherein generating the fault signal is performed using logic control circuitry for driving the pair of input path selection switches.

27. (New) A method according to Claim 26, wherein the integrated circuit further comprises a register for storing the numerical value of the internally generated analog reference signal; and a comparator having a first input connected to the register for receiving the numerical value of the internally generated analog reference signal, and a second input connected to the analog-to-digital converter for receiving the numerical value of the externally generated analog signal; and a pair of output path selection switches coupling an output of the analog-to-digital converter either to an input of the register during the pre-sampling phase of the analog-to-digital converter or to the second input of the comparator during the successive operating phase of the analog-to-digital converter; and the logic control circuitry for driving the pair of output path selection switches.

28. (New) A method according to Claim 27, wherein an output of the comparator provides the fault signal.

29. (New) A method according to Claim 27, wherein the logic control circuitry drives the pair of input path selection switches in an opposing phase, and drives the pair of output path selection switches in an opposing phase.

30. (New) A method according to Claim 27, wherein the comparator defines a range of values between two thresholds for comparing with the numerical value of the externally generated analog signal.

31. (New) A method according to Claim 27, wherein the integrated circuit further comprises a counter coupled to an output of the comparator for providing the fault signal when the comparator verifies that the numerical value of the externally generated analog signal is equal to the numerical value of the internally generated analog reference signal for a certain number of successive samples of the externally generated analog input signal.

32. (New) A method according to Claim 24, wherein the electrical connection is an automobile so that the method is part of an auto-diagnostic test performed by the automobile.